IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Eliyahou Harari, Robert D. Norman and Sanjay Mehrotra		
Assignee:	SanDisk Corporation		
Title:	Flash EEPROM System		
Serial No.:	09/867,836	Filing Date:	May 30, 2001
Examiner:	A. Tran	Group Art Unit:	2824
Docket No.:	11587 M-10187-43C US		

6th Election

San Francisco, California
October 8, 2001

BOX AMENDMENTS
COMMISSIONER FOR PATENTS
Washington, D. C. 20231

10/17/01 E Brown

RESPONSE TO REQUIREMENT FOR RESTRICTION AND PRELIMINARY AMENDMENT

Dear Sir:

In response to the Office Action dated September 10, 2001, in the above-identified patent application, method claims 81-82, 84, 86-90 and 93 of group III are hereby elected for examination.

However, since claim 81 is in independent form and all of claims 82-94 are dependent thereon, it is requested that all of the method claims 81-94 be examined together in this application. Contrary to what is stated in the Office Action, claim 81 is not limited to two-level memory cells. Nor is it limited to multi-level (more than two level) operation. Rather, it is generic to both two-level and multi-level operation. All of dependent claims 86-90 are similarly generic to both. Only dependent claims 82 and 84, and claims dependent upon them, are limited to two-state operation. Similarly, only dependent claims 83 and 85, and their dependent claims, are limited to multi-state operation. It therefore appears appropriate to examine all of claims 81-94 together. Alternatively, even if only the claims designated in group III are examined, all of claims 81-94 should be allowed in this application if the single independent claim 81 is found to be allowable.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979

PRELIMINARY AMENDMENT

Please add the following new claims, which are dependent upon the elected group of claims:

95. (New) The method of claim 81, where resetting said blocks includes selecting said number of blocks less than all of the blocks in the array by electronically tagging said number of blocks, and then simultaneously applying reset voltage conditions to the memory cells within all of the selected blocks.

96. (New) The method of any one of claims 81, 82 or 83, wherein the appropriate voltage conditions are applied to the plurality of memory cells within one of the reset blocks in accordance with a chunk of user data stored in a cache memory in response to additional space for new user data from a host being required in the cache memory.

B1

97. (New) The method of claim 96, carried out on a single integrated circuit chip.

98. (New) The method of claim 96, wherein there are exactly two threshold level ranges.

99. (New) The method of claim 96, wherein there are more than two threshold level ranges.

100. (New) The method of any one of claims 81, 82 or 83, wherein the memory system is enclosed in a card having a connector adapted to be removeably connected with a host system.

LAW OFFICES OF
SKJERVEN MORRILL
MACPHERSON LLP

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 453-9200
FAX (408) 453-7979